IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Jerry T Rahll
Serial No.:	10/052952	Group Art Unit:	2874
Filed:	January 17, 2002	Docket:	1303.034US1
Title:	THREE-DIMENSIONAL PHOTONIC CRYSTAL WAVEGUIDE STRUCTURE AND METHOD		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 4/8/04

By _____
Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of April, 2004.

Name Amy Moriarty

Signature _____

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 1 of 8

Attorney Docket No: 1303.034US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US20020001965	01/03/2002	Forbes, Leonard	438	734	07/22/1997
	US20020070421	06/13/2002	Ashburn, Stanton P.	257	510	02/08/2002
	US20020185686	12/12/2002	Christiansen, Silke H., et al.	257	347	04/03/2002
	US20030227072	12/11/2003	Forbes, Leonard	257	616	06/10/2002
	US20030027406	02/06/2003	Malone, Farris D.	438	471	08/01/2001
	US20030201468	10/30/2003	Christiansen, H., et al.	257	200	04/30/2003
	US20030218189	11/27/2003	Christiansen, Silke H., et al.	257	200	11/19/2002
	US-4,241,359	12/23/1980	Izumi, Katsutoshi , et al.	257	386	03/02/1978
	US-4,589,928	05/20/1986	Dalton, John V.	438	142	08/21/1984
	US-4,717,681	01/05/1988	Curran, Patrick A.	438	314	05/19/1986
	US-5,426,061	06/20/1995	Sopori, Bhushan L.	438	475	09/06/1994
	US-5,443,661	08/22/1995	Oguro, Shizuo , et al.	148	33.5	07/27/1994
	US-5,461,243	10/24/1995	Ek, Bruce A., et al.	257	190	10/29/1993
	US-5,646,053	07/08/1997	Schepis, Dominic J.	438	402	12/20/1995
	US-5,661,044	08/26/1997	Holland, Orin W., et al.	438	766	06/15/1995
	US-5,691,230	11/25/1997	Forbes, Leonard	437	62	09/04/1996
	US-5,759,898	06/02/1998	Ek, Bruce , et al.	438	291	12/19/1996
	US-5,773,152	06/30/1998	Okonogi, Kensuke	428	446	10/13/1995
	US-5,789,859	08/04/1998	Watkins, Charles M., et al.	313	495	11/25/1996
	US-5,840,590	11/24/1998	Myers Jr., Samuel M., et al.	438	471	12/01/1993
	US-5,879,996	03/09/1999	Forbes, Leonard	438	289	09/18/1996
	US-5,963,817	10/05/1999	Chu, Jack O., et al.	438	410	10/16/1997
	US-5,997,378	12/07/1999	Dynka, Danny , et al.	445	25	07/29/1998
	US-6,001,711	12/14/1999	Hashimoto, Takasuke	438	473	03/09/1998
	US-6,022,793	02/08/2000	Wijaranakula, Witawat , et al.	438	473	10/21/1997
	US-6,054,808	04/25/2000	Watkins, Charles M., et al.	313	495	01/26/1999
	US-6,083,324	07/04/2000	Henley, Francois J., et al.	148	33.2	02/19/1998
	US-6,093,623	07/25/2000	Forbes, Leonard	438	455	08/04/1998
	US-6,093,624	07/25/2000	Letavic, Theodore J., et al.	438	462	12/23/1997

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 2 of 8

Attorney Docket No: 1303.034US1

	US-6,127,777	10/03/2000	Watkins, Charles M., et al.	313	554	07/31/1998
	US-6,172,456	01/09/2001	Cathey, David A., et al.	313	495	04/05/1999
	US-6,174,784	01/16/2001	Forbes, Leonard	438	405	11/14/1997
	US-6,204,145	03/20/2001	Noble, Wendell P.	438	412	08/07/1998
	US-6,228,694	05/08/2001	Doyle, Brian S., et al.	438	199	06/28/1999
	US-6,251,751	06/26/2001	Chu, Jack O., et al.	438	439	04/13/1999
	US-6,274,460	08/14/2001	Delgado, Jose A., et al.	438	476	06/17/1999
	US-6,309,950	10/30/2001	Forbes, Leonard	438	455	03/23/2000
	US-6,315,826	11/13/2001	Muramatsu, Satoru	117	95	06/22/2000
	US-6,338,805	01/15/2002	Anderson, Gary L.	216	89	07/14/1999
	US-6,339,011	01/15/2002	Gonzalez, Fernando , et al.	438	473	03/05/2001
	US-6,368,938	04/09/2002	Usenko, Alexander Y.	438	407	06/07/2000
	US-6,376,336	04/23/2002	Buynoski, Matthew S.	438	476	02/01/2001
	US-6,377,070	04/23/2002	Forbes, Leonard	326	41	02/09/2001
	US-6,391,738	05/21/2002	Moore, John T.	438	402	12/20/2000
	US-6,423,613	07/23/2002	Geusic, Joseph	438	455	11/10/1998
	US-6,424,001	07/23/2002	Forbes, Leonard , et al.	257	315	02/09/2001
	US-6,444,534	09/03/2002	Maszara, Witold P.	438	311	01/30/2001
	US-6,448,601	09/10/2002	Forbes, Leonard , et al.	257	302	02/09/2001
	US-6,478,883	11/12/2002	Tamatsuka, Masaro , et al.	148	33.2	04/18/2000
	US-6,496,034	12/17/2002	Forbes, Leonard , et al.	326	041	02/09/2001
	US-6,531,727	03/11/2003	Forbes, Leonard , et al.	257	302	02/09/2001
	US-6,538,330	03/25/2003	Forbes, Leonard	257	777	03/23/2000
	US-6,559,491	05/06/2003	Forbes, Leonard , et al.	257	296	02/09/2001
	US-6,566,682	05/20/2003	Forbes, Leonard	257	51	02/09/2001
	US-6,582,512	06/24/2003	Geusic, Joseph E., et al.	117	3	05/22/2001
	US-6,593,625	07/15/2003	Christiansen, Silke H., et al.	257	347	04/03/2002
	US-6,597,203	07/22/2003	Forbes, Leonard	326	98	03/14/2001
	US-6,630,713	10/07/2003	Geusic, Joseph	257	347	02/25/1999
	US-6,649,476	11/18/2003	Forbes, Leonard	438	268	02/15/2001

EXAMINER **DATE CONSIDERED**

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 3 of 8

Attorney Docket No: 1303.034US1

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]
	EP-434984	09/03/1991	Lindberg, Keith J., et al.	H01L	21/322	
	WO-WO02097982	12/05/2002	Pavio, Anthony M., et al.	H03 G	3/10	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		"Cornell Demonstrates a Universal Substrate", Compound Semiconductor, 3(2), (March/April 1997),27-29	
		ABE, T , "Silicon Wafer-Bonding Process Technology for SOI Structures", Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, (1990),853-856	
		AUBERTON-HERVE, A J., "SOI: Materials to Systems", International Electron Devices Meeting. Technical Digest, (1996),3-10	
		AUTUMN, KELLAR , et al., "Adhesive force of a single gecko foot-hair", Nature, 405(6787), (June 2000),681-685	
		AUTUMN, KELLAR , et al., "Evidence for van der Waals adhesion in gecko setae.", Proceedings of the National Academy of Science U S A.; 99(19), (September 17, 2002),12252-6	
		BAGINSKI, T. A., "Back-side germanium ion implantation gettering of silicon", Journal of the Electrochemical Society, 135(7), Dept of Electrical Engineering, Auburn Univ, AL,(July 1988),1842-3	
		BELFORD, RONA E., "Performance-Augmented CMOS Using Back-End Uniaxial Strain", IEEE Device Research Conference, (2002),41-42	
		BERTI, M. , "Composition and Structure of Si-Ge Layers Produced by Ion Implantation and Laser Melting", Journal of Materials Research, 6(10), (October 1991),2120-2126	
		BERTI, M. , "Laser Induced Epitaxial Regrowth of Si]-xGex/Si Layers Produced by Ge Ion Implantation", Applied Surface Science, 43, (1989),158-164	
		BIALAS, F. , et al., "Intrinsic Gettering of 300 mm CZ Wafers", Microelectronic Engineering, 56(1-2), (May 2001),157-63	
		BIEVER, CELESTE , "Secret of 'strained silicon' revealed: behind closed doors, Intel has perfected a novel way to improve chip performance.", New Scientist, 180(i2426-2428), (December 20, 2003),27	
		BINNS, M. J., et al., "The Realization of Uniform and Reliable Intrinsic Gettering in 200mm P- & P/P Wafers for a Low Thermal Budget 0.18 mu m Advanced CMOS Logic Process", Diffusion and Defect Data Pt.B: Solid State Phenomena, 82-84, (2001),387-92	
		BRONNER, G. B., et al., "Physical Modeling of Backside Gettering", Impurity Diffusion and Gettering in Silicon Symposium, Sponsor: Mater. Res. Soc, Nov 1984, Boston, MA,(1985),27-30	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 4 of 8

Attorney Docket No: 1303.034US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		BROWN, CHAPPELL , "Bonding twist hints at universal substrate", EETimes, (1997),2 pages	
		BRUEL, M , et al., "Smart-Cut: a new silicon on insulator material technology based on hydrogen implantation and wafer bonding", Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers), 36(3B), (1997),1636-1641	
		CHEN, XIANGDONG , et al., "Vertical P-MOSFETs with heterojunction between source/drain and channel", IEEE Device Research Conference, (2000),25-26	
		CHILTON, B T., et al., "Solid phase epitaxial regrowth of strained Si(1-x)Ge(x)/Si strained layer structures amorphized by ion implantation", Applied Physics Letters, 54(1), (January 2, 1989),42-44	
		CHOE, K. S., et al., "Minority-Carrier Lifetime Optimization in Silicon MOS Devices by Intrinsic Gettering", Journal of Crystal Growth, 218(2-4), (September 2000),239-44	
		CLARK, DON , et al., "Intel unveils tiny new transistors: Process handles circuits 1/2000th the width of a human hair", The Wall Street Journal, (August 13, 2002),3 pages	
		CLIFTON, P A., et al., "A process for strained silicon n-channel HMOSFETs", ESSDERC'96. Proceedings of the 26th European Solid State Device Research Conference, (September 1996),519-22	
		DUBBELDAY, W B., et al., "Oscillatory strain relaxation in solid phase epitaxially regrown silicon on sapphire", Proceedings of the First International Workshop Lattice Mismatched Thin Films, (September 13-15, 1998),13-17	
		FISCHETTI, M V., et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys", Journal of Applied Physics, 80(4), (August 15, 1996),2234-2252	
		FOURNEL, F , et al., "Ultra High Precision Of The Tilt/Twist Misorientation Angles In Silicon/Silicon Direct Wafer Bonding", Abstract - Electronic Materials Conference, (June 2002),9	
		GARCIA, G A., et al., "High-quality CMOS in thin (100 nm) silicon on sapphire", IEEE Electron Device Letters, 9(1), (January 1988),32-34	
		GODBOLE, H. , et al., "An Investigation of Bulk Stacking Faults in Silicon Using Photocapacitance Transient Spectroscophy", Materials Letters, 8(6-7), Dept of Electr & Comput Engr, Oregon State Univ, Corvallis OR,(July 1989),201-3	
		GONG, S. S., et al., "Implantation Gettering in Silicon", Solid-State Electronics, 30(2), (February 1987),209-11	
		GRAF, D. , et al., "300 mm epi pp- wafer: is there sufficient gettering?", High Purity Silicon VI. Proceedings of the Sixth International Symposium (Electrochemical Society Proceedings Vol. 2000-17) (SPIE Vol.4218), (2000),319-30	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 5 of 8

Attorney Docket No: 1303.034US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		HADDAD, H. , et al., "Carbon Doping Effects on Hot Electron Trapping", 28th Annual Proceedings. Reliability Physics 1990, (March 1990),288-9	
		HADDAD, H. , et al., "Electrical Activity of Bulk Stacking Faults in Silicon", Materials Letters, 7(3), Hewlett-Packard Northwest Integrated Circuits Div, Corvallis OR,(September 1988),99-101	
		HARENDT, CHRISTINE , "Silicon on Insulator Material by Wafer Bonding", Journal of Electronic Materials, 20(3), (March 1991),267-77	
		IYER, S S., "Separation by Plasma Implantation of Oxygen (SPIMOX) operational phase space", IEEE trans. on Plasma Science, 25, (1997),1128-1135	
		KALAVADE, PRANAV , et al., "A novel sub-10 nm transistor", 58th DRC. Device Research Conference. Conference Digest, (June 19-21, 2000),71-72	
		KANG, J. S., et al., "Gettering in Silicon", Journal of Applied Physics, 65(8), Center for Solid State Electron Res., Arizona State Univ., Tempe, AZ,(April 15, 1989),2974-85	
		KOSTRZEWA, M , et al., "Testing the Feasibility of strain relaxed InAsP and InGaAs compliant substrates", EMC 2003 International Conference Indium Phosphide and Related Materials. Conference Proceedings, Other authors: G. Grenet et al,(6/2003),8-9	
		KUNG, C. Y., et al., "The effect of carbon on oxygen precipitation in high carbon CZ silicon crystals", Materials Research Bulletin, 18(12), Silicon Materials Div., Fairchild Camera & Instrument Corp, Healdsburg, CA,(December 1983),1437-41	
		LASKY, J. B., "Wafer Bonding for Silicon-on-Insulator Technologies", Applied Physics Letters, 48(1), (January 6, 1986),78-80	
		LI, Y. X., et al., "New intrinsic gettering process in Czochralski-silicon wafer", 6th International Conference on Solid-State and Integrated Circuit Technology. Proceedings, 1(1), (2001),277-9	
		LOO, Y L., et al., "Contact Printing With Nanometer Resolution", Device Research Conference, (June 2002),149-150	
		LU, D, , "Bonding Silicon Wafers by Use of Electrostatic Fields Followed by Rapid Thermal Heating", Materials Letters, 4(11), (October 1986),461-464	
		MIZUNO, T , et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS Electron/Hole Mobility Enhancement", 2000 Symposium on VLSI Technology. Digest of Technical Papers, (2000),210-211	
		MORAN, PETER , "Strain Relaxation in Wafer-Bonded SiGe/Si Heterostructures Due to Viscous Flow of an Underlying Borosilicate Glass", Electronic Materials Conference, Santa Barbara, June 2002, Abstract,(June 2002),Pgs. 8-9	
		MUMOLA, P. B., et al., "Recent advances in thinning of bonded SOI wafers by plasma assisted chemical etching", Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications, (1995),28-32	

EXAMINER **DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 6 of 8

Attorney Docket No: 1303.034US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		NAYAK, D.K. , "High performance GeSi quantum-well PMOS on SIMOX", International Electron Devices Meeting 1992. Technical Digest, (1992),777-80	
		O'NEILL, A G., et al., "High speed deep sub-micron MOSFET using high mobility strained silicon channel", ESSDERC '95. Proceedings of the 25th European Solid State Device Research Conference, (September 1995),109-12	
		OMI, HIROO , et al., "Semiconductor Surface with Strain Control", http://www.brl.ntt.co.jp/J/kouhou/katsudou/report00/E/report04_e.html,	
		OR, B S., et al., "Annealing effects of carbon in n-channel LDD MOSFETs", IEEE Electron Device Letters, 12(11), Dept of Electrical & Computing Engr, Oregon State Univ, Corvallis OR,(November 1991),596-8	
		OUYANG, Q , et al., "Bandgap Engineering in Deep Submicron Vertical pMOSFETs", IEEE 58th DRC. Device Research Conference. Conference Digest, (2000),27-28	
		PAINE, D. C., "The Growth of Strained Si]-xGex Alloys on (100) Silicon Using Solid Phase Epitaxy", Journal of Materials Research, 5(5), (May 1990),1023-1031	
		PEOPLE, R. , "Calculation of critical layer thickness versus lattice mismatch for GexSi1-x/Si strained-layer heterostructures", Applied Physics Letters, 47(3), (August 1, 1985),322-4	
		RIM, KERN , et al., "Fabrication and analysis of deep submicron strained-Si n-MOSFET's", IEEE Transactions on Electron Devices, 47(7), (July 2000),1406-1415	
		RIM, KERN , et al., "Strained Si NMOSFETs for High Performance CMOS Technology", 2001 Symposium on VLSI Technology. Digest of Technical Papers, (2001),59-60	
		RIM, KERN , et al., "Transconductance enhancement in deep submicron strained Si n-MOSFETs", International Electron Devices Meeting 1998. Technical Digest, (1998),707-710	
		RUBIN, L , et al., "Effective gettering of oxygen by high dose, high energy boron buried layers", 1998 International Conference on Ion Implantation Technology. Proceedings, 2(2), (1998),1010-13	
		SATO, T , "Trench transformation technology using hydrogen annealing for realizing highly reliable device structure with thin dielectric films", 1998 Symposium on VLSI Technology Digest of Technical Papers, (1998),206-7	
		SUGIYAMA, N , et al., "Formation of strained-silicon layer on thin relaxed-SiGe/SiO/sub 2//Si structure using SIMOX technology", Thin Solid Films, 369(1-2), (July 2000),199-202	
		TAKAGI, SHIN-ICHI , "Strained-Si- and SiGe-On-Insulator (Strained-SOI and SGOI) MOSFETs for High Performance/Low Power CMOS Application", IEEE Device Research Conference, 2002. 60th DRC. Conference Digest, (2002),37-40	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 7 of 8

Attorney Docket No: 1303.034US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		TAN, T. Y., et al., "Intrinsic gettering by oxide precipitate induced dislocations in Czochralski Si", Applied Physics Letters, 30(4), IBM System Products Div., Essex Junction, VT,(February 15, 1977),175-6	
		VERDONCKT-VANDEBROEK,, SOPHIE , et al., "SiGe-Channel Heterojunction p-MOSFET's", IEEE Transactions on Electron Devices, 41(1), (January 1994),90-101	
		WELSER, J , et al., "Strain dependence of the performance enhancement in strained-Si n-MOSFETs", IEEE International Electron Devices Meeting 1994. Technical Digest, (December 11-14, 1994),373-376	
		WHITWER, F. D., et al., "DLTS characterization of precipitation induced microdefects", Materials Issues in Silicon Integrated Circuit Processing Symposium, (April 1986),53-57	
		WIJARANAKULA, W. , et al., "Effect of Pre- and Postepitaxial Deposition Annealing on Oxygen Precipitation in Silicon", Journal of Materials Research, 1(5), Dept of Electr & Comput Eng, Oregon State Univ, Corvallis, OR,(September-October 1986),698-704	
		WIJARANAKULA, W. , et al., "Effect of preanneal heat treatment on oxygen precipitation in epitaxial silicon", Materials Issues in Silicon Integrated Circuit Processing Symposium, (April 1986),139-44	
		WIJARANAKULA, W. , et al., "Internal Gettering Heat Treatments and Oxygen Precipitation in Epitaxial Silicon Wafers", Journal of Materials Research, 1(5), Dept of Electr & Comput. Eng, Oregon State Univ., Corvallis, OR,(September-October 1986),693-7	
		WIJARANAKULA, W. , et al., "Oxygen precipitation in p/p+(100) epitaxial silicon material", Journal of the Electrochemical Society, 134(9), SEH America, Inc., Mater. Characterization Lab., Vancouver, WA,(September 1987),2310-16	
		XUAN, PEIQI , et al., "60nm Planarized Ultra-thin Body Solid Phase Epitaxy MOSFETs", IEEE Device Research Conference, Conference Digest. 58th DRC, (June 19-21, 2000),67-68	
		YANG, D. , et al., "Intrinsic Gettering in Nitrogen Doped Czochralski Crystal Silicon", High Purity Silicon VI. Proceedings of the Sixth International Symposium (Electrochemical Society Proceedings Vol. 2000-17) (SPIE Vol.4218), (2000),357-61	
		YANG, DEREN , et al., "Nitrogen in Czochralski Silicon", 2001 6th International Conference on Solid-State and Integrated Circuit Technology. Proceedings, 1(1), (2001),255-60	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 8 of 8

Attorney Docket No: 1303.034US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		YIN, HAIZHOU , "High Ge-Content Relaxed Sil-xGex Layers by Relaxation on Complaint Substrate with Controlled Oxidation", Electronic Materials Conference, Santa Barbara, June 2002, (June 2002),8	
		ZHU, Z H., et al., "Wafer bonding and its application on compliant universal (CU) substrates", Conference Proceedings, 10th Annual Meeting IEEE Lasers and Electro-Optics Society, (November 10-13, 1996),31	
		ZHU, Z H., et al., "Wafer bonding technology and its applications in optoelectronic devices and materials", IEEE Journal of Selected Topics in Quantum Electronics, (June 1997),927 - 936	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached